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DIGITAL SWITCHING NOISE REDUCTION METHODS IN MIXED SIGNAL INTEGRATED CIRCUITS

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ABSTRACT

In mixed-signal integrated circuits (ICs) analog and digital parts share the same substrate. When digital circuits are switching they generate noise that is spread through the silicon substrate to other circuits. Substrate noise is a major problem in mixed-signal ICs where it seriously degrades the performance of sensitive analog circuits.

1. INTRODUCTION

1.1 Reduction of Digital Switching Noise.

1.1.1 Multiple Power Supply Interconnects

Inductance of the power supply from off chip to on chip can be reducing multiple power supply power**.**How the total inductance is affected if, e.g., two pairs of interconnects are used instead of one pair of interconnects. If the distance between the two pairs of interconnects is large, the mutual inductance can be neglected. Consequently, the total effective inductance is simply the half ofthe original. In Fig. 1.1, two pairs of interconnects that are placed adjacent to each other are shown. The distance between the interconnects is *d* and their radius is *a*. The interconnects labeled 1 and 3 are connected so that they have the same current direction. The interconnects labeled 2 and 4 are connected so that the currents have the opposite direction with respect to interconnects 1 and 3. Owing to the symmetry the currents in the two outermost interconnect are equal. For the same reason, the currents in the two innermost interconnects are equal. Hence, we have two closed current loops with the internal wire

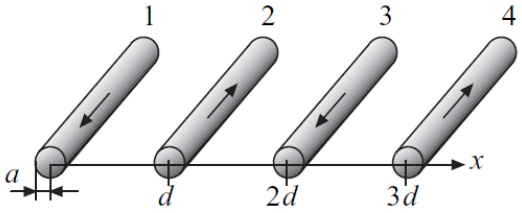

Figure 1.1: Four wires running in parallel

distances of *d* and 3*d*, respectively. The self-inductance per length unit of the inner current path and the outer current path are denoted L'_1 and L'_2 respectively. Hence,

$$L'_1 = {}^{\mu_0}/_{\pi}\left(\frac{1}{4} + In(\frac{d}{a} - 1)\right) \quad 1.1$$

And

$$L'_2 = {}^{\mu_0}/_{\pi}\left(\frac{1}{4} + In(\frac{3d}{a} - 1)\right) \quad 1.2$$

Owing to the symmetry, the mutual inductance per unit length of the two loops may be calculated as

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$$L'_{12} = \frac{1}{I}\int_{s12} B.ds'_{12} = -\frac{\mu_0}{\pi}\int_{(d+a)}^{(2d-a)} \frac{1}{x}\,dx = -\frac{\mu_0}{\pi} In\left(\frac{2d/a - 1}{d/a + 1}\right) \quad 1.3$$

The effective inductance per unit length of the paths are

$$L'_{1eff} = \frac{\mu_0}{\pi}\left[\frac{1}{4} + In\left(\frac{d}{a} - 1\right) - In\left(\frac{2d/a - 1}{d/a + 1}\right)\right] \quad 1.4$$

and

$$L'_{2eff} = \frac{\mu_0}{\pi}\left[\frac{1}{4} + In\left(\frac{3d}{a} - 1\right) - In\left(\frac{2d/a - 1}{d/a + 1}\right)\right] \quad 1.5$$

The effective inductance of the four wires corresponds to two inductors in parallel with the value of L'_{1eff} and L'_{2eff}, respectively. Hence, the effective inductance per unit length of the four interconnects is

$$L'_{eff} = \frac{L'_{eff}\, L'_{eff}}{L'_{eff} + L'_{eff}} \quad 1.6$$

Another configuration is shown in Fig. 1.2. In this case, the interconnects labeled 1 and 2 are connected so that they have the same current direction. The interconnects labeled 3 and 4 are connected so that their currents have the opposite direction with respect to the currents in wire 1 and 2. We cansolve the problem in the same way as the previous one, exceptthat

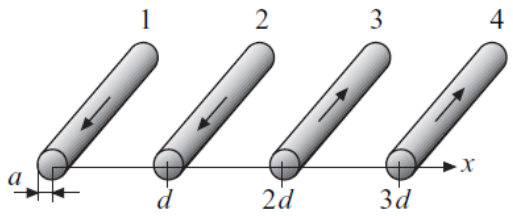

Figure 1.2: Four wires running in parallel.

We have to consider that the current direction of the inner loop is changed. Therefore, we can reuse the previous calculations in (1.1) to (1.6) with the exception that the sign in (1.3) is changed.

1.1.2 Double Bonding

One technique aiming at reducing the impedance between on-chip and offchip is the double bonding. Instead of using one bonding wire from the on chip pad to the off-chip interconnect two bonding wires are used, which is illustrated in Fig. 1.3(a) and Fig. 1.3(b), respectively.In two metal areas, with a ground plane beneath, are connected with bonding wires. In this case the ground plane serves as a current return path, which significantly reduces the inductance of the double bonding. On the other hand, in the case of conventionally connected power supply lines, the current path is normally through the bonding wires. Hence, the effectiveness of using double bonding for a power supply may besmall. However, with double bonding the parasitic resistance is reduced to the half. This can be beneficial especially for high frequencies, where the resistance of a conductor increases with due $\sqrt{f}$ to the skin effect. A thick bonding wire may also be used for the same purpose.

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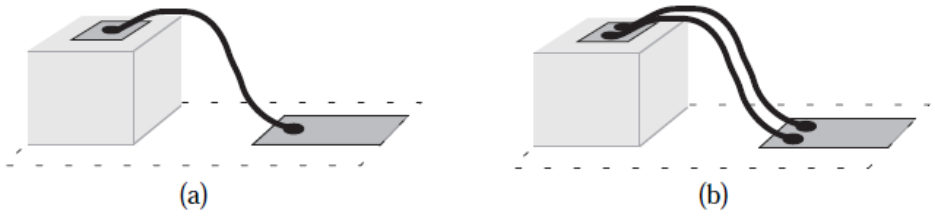

Figure 1.3: (a) Illustration of single bonding and (b) double bonding.

Commonlybeen added as a single capacitor. Nowadays with circuits operating at high frequencies it is preferable to distribute the decoupling capacitors over the whole chip are.
The decoupling may be designed as an individual cell in a standard cell library or it may be included within each standard cell.

1.1.4 Reduction of Main Peak in Power Supply Impedance

The resonance frequency of the on-chip power supply lines is seen as a peak in the impedance frequency domain. In a simple circuit is used to eliminate the peak in impedance at the resonance frequency. The circuit consists of a resistor, a capacitor, and an inductance in series. The inductance and the capacitor are chosen so that the resonance frequency is placed at the same frequency as the impedance peak of the original power supply. In this way the original impedance peak can be reduced. The inductance is implemented by bonding wires and the resistor and capacitor are placed off chip. The resistor in the circuit makes it possible to avoid new peaks in the impedance characteristic by selecting a proper resistance.

1.1.5 Reduced Supply Bounce CMOS Logic

In reduced supply bounce (RSB) CMOS logic is proposed. The digital circuits are implemented in static CMOS together with a simple circuit for reducing SSN on supply lines. The circuit is illustrated in Fig. 1.4, where the transistors in series with the power supply lines are serving as resistors to intense the SSN. The capacitors *C*1 and *C*2 serve as decoupling to reduce theSSN.Measurements on a test chip show a noise reduction of 67% when compared to conventional static CMOS.

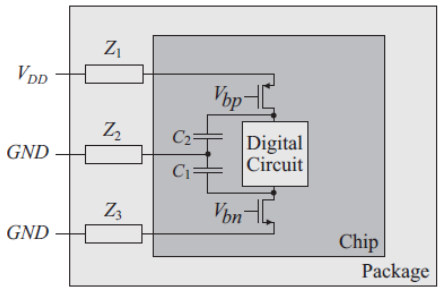

Figure 1.4: Reduced supply bounce CMOS logic.

1.1.6 Clock Skew

In synchronous digital circuits the clock signal synchronizes the operation of the clocked elements (e.g., registers). On the triggering clock edge each output of the registers are updated and the following logic starts to evaluate simultaneously, resulting in SSN. In a clock net is divided into four clock regions where each region has its individual and dedicated delay (i.e., clock skew) from the nominal clock, which is illustrated in Fig. 1.5. In this way the triggering clock edge appears at different time instances in the different regions preventing the switching of the circuits in respective region to start simultaneously. With this method the resulting current peak can be smoothened, which results in a lower SSN. Measurements on a test chip in show a reduction of SNN with more than a factor of 2. Care must be taken with signals that originate from one clock domain and ends in anotherdomain to prevent the

timing window of the registers from being violated. If there is a risk of violating the hold time of the registers, inserting extra delay in the logic can prevent the hold time from being violated. The technique may be effective if the timing constraints allow it to be used.

1.1.7 Modulation of Clock Frequency

When SSN is analyzed in the frequency domain the clock frequency and the harmonics are clearly seen. If the clock frequency is varied a smallfraction, the energy at the clockfrequencyand its harmonics are spread over a wider bandwidth.This approach yields lower,

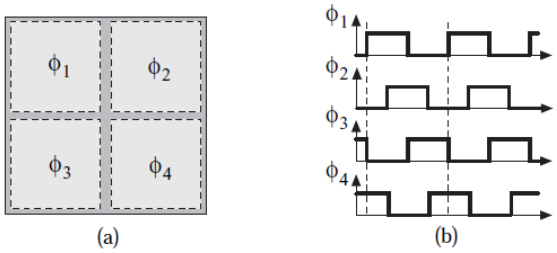

Figure 1.5: (a) A chip divided into four clock regions, and (b) four clock signalswith same frequency, but different phases.

but wider peaks in the frequency domain which is illustrated for the clock frequency and it first harmonic in Fig. 1.6. In the clock on a PCB is frequency modulated to reduce the radiated emission. The measured reduction of the peaks in the frequency domain of the radiated emission was up to 13 dB. The frequency deviation of the clock was up to 2.5%. Note that the total spectral power is not changed, but more distributed on the frequency axis. In a frequency modulated clock is used together with intentional clock skew to reduce the spectral peaks on the on-chip ground. Simulation results show attenuation with more than 26 dB. Using only the frequency modulation, the attenuation was more than 14 dB.

1.1.8 Timing and Sizing of Output Buffers

Output buffers are often main contributors to. When an output change value the current peak can be high and the correspondingdI/dt can be large yielding a high SSN. To prevent output buffers from switching simultaneously, they can be designed with different propagation delays from the first stage to the final stage in each buffer. This approach reduces the maximaldI/dt . The difference in timing of the outputs must be within a certain bound so that the circuit can communicate properly with other circuits. It is also important that the output buffers are not oversized in terms of propagation delay and rise and fall times that are shorter than necessary. Oversized buffers result in larger area, higher power consumption and more SSN when compared to properly sized buffers.

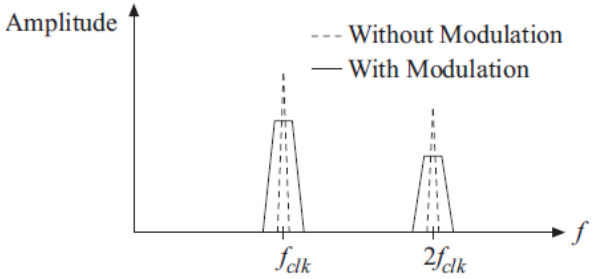

Figure 1.6: Illustration of frequency spectrum with and without frequency modulation of the clock.

1.1.9 Reduced Power Supply Voltage

Power supply voltage scaling is commonly used to lower the powerconsumption of digital circuits. Reducing the power supply voltage reduces the effective gate voltages giving smaller drain currents. This yields longer rise and fall times on the gate inputs and therefore a decrease in peak current and.Hence, a reduced power supply voltage results in a reduced SSN. In a mixed-signal test chip is evaluated, which consist of a digital circuit and analog comparators. The experimental results show that scaling down the power supply voltage effectively reduce the

substrate noise, as expected considering the drain currents of the transistors. Another benefit of using a reduced supply voltage is the reduced dynamic power consumption, which is in proportion to Vdd2 The static power consumption also decreases. However, the cost is a decreased throughput, which may be compensated by, e.g., pipelining or interleaving. Pipelining and interleaving both require extra hardware that may contribute to the noise. Hence, the gain of decreasing the power supply voltage on the substrate noise depends on what changes that must be done in the architecture to fulfill the requirement on throughput.

1.1.10 Constant Current Logic

In constant current logic the circuits are designed with the target on making the power supply currents as constant as possible. The main idea is to steercurrents so that only the paths change but not the magnitude of the currents.In practice, a constant current is impossible to achieve due to that the currentscannot be perfectly balanced during the switching of the current paths. In Fig. 1.7 current steering logic (CSL), current balanced logic (CBL),complementary current balanced logic (C-CBL), and folded source coupledlogic (FSCL) are shown. In simulations are made on extracted layouts ofconventional static CMOS logic, current steering logic (CSL) circuit, currentbalanced logic (CBL), and complementary current balanced logic (C-CBL).An example shows that the relative difference between the circuits depends on the inductance in the power supply lines. For a small inductance the noise of CSL and CNL are lower than of CMOS. For a larger inductance CSL becomes noisier than both CBL and static CMOS. With the CMOS circuit as reference and assuming a power supply inductance of 10nH, CBL results in the best noise reduction corresponding to 55%. C-CBL reduces the noise with 43% while CSL reduces the noise with 12%. For a power supply inductance below 1nH, CCBL reduces the noise with 50% while CSL and CBL reduce the noise with 20%. In measurements on a manufactured test chip indicated a noise reduction up to 55% for CBL when compared to CMOS, which is in good agreement with the simulation results in. In simulation results indicate that the use of FCSL results in power supply current spikes of two orders of magnitude smaller than the current spikes in CMOS. However, SSN is mainlydetermined by the value of dI/dt and not the peak-to-peak value of the current spike.

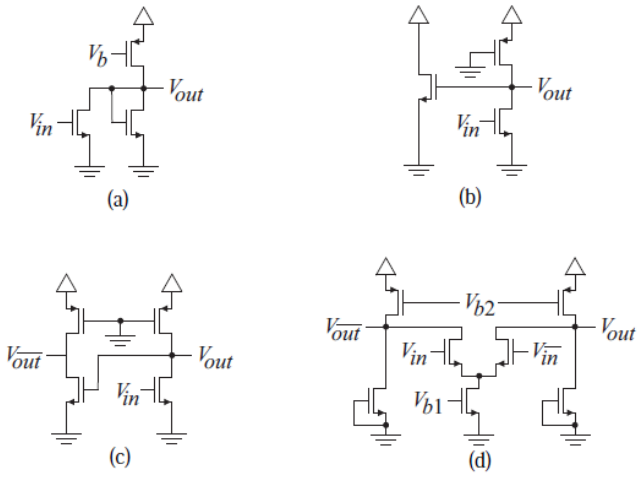

Figure 1.7: (a) Current steering logic (CSL), (b) current balanced logic (CBL), (c) complementary current balanced logic C-CBL, and (d) folded source coupled logic (FSCL).

Therefore, it is hard to draw conclusions on how much the reduction of the current spikes in FSCL reduces the SSN. The cost of the noise reduction using constant current logic may be high in terms of high static power consumption, which may make the technique less suitable for battery powered products. The constant current logic circuits also tend to occupy somewhat larger silicon area than, e.g., static CMOS. However, if increased power consumption and somewhat increased area are afforded then constant current logic may be suitable.

1.1.12 Asynchronous Circuits

In asynchronous circuits no clock is used. Asynchronous circuits have a favorable switching noise compared with synchronous circuits since the switching in asynchronous circuits is more distributed in time than in synchronous circuits. This results in a power supply current with less noise. In Philips 80C51 processor was implemented in an

asynchronous and a synchronous version in the same CMOS technology. The circuit designed in asynchronous logic yielded up to 30 dB smaller peaks in the frequency spectra of the power supply current compared with the circuit built using conventional synchronous logic. However, the design of asynchronous circuits is not as well supported as the design of synchronous circuits. Therefore, designing asynchronous circuits can be challenging from a designers point of view.

2. REDUCTION OF COUPLING

1.2.1 Separate Power Supply Lines

The power supply lines of digital circuits do always suffer from some voltage fluctuations (i.e., SSN) during the switching. To prevent the switching noise from being directly coupled to other circuits, it is common to use separate power supply lines for analog and digital circuits as illustrated in Fig. 1.08. Even if the power supply lines to an analog and a digital circuit originate from the same off-chip power supply source, it is still efficient to separate them on chip from a noise reduction point of view. This is due to that the package impedance is located in between the common nodes outside the chip and the separate nodes on chip. Therefore, the package impedance causes the power supplies to be less coupled for high frequencies. In the test chips used in this thesis work, separate power supply lines are used for the digital and the analog circuits. If separating power supplies the designer must consider all the connections between the different power supply domains. When a signal is transmitted between two circuits with separate grounds it is important that the ground voltages do not differ too much in voltage levels. If the ground voltages differ, e.g., during a transition, then the signal may be misinterpreted and the receiving circuit may malfunction. The increased impedance in the current return path of the signal may slow down the propagation delay significantly if a common ground is divided into two separate grounds. In simulations on a circuit level, models of the impedance between separated ground regions must be included if there are high-speed signals connected between them.

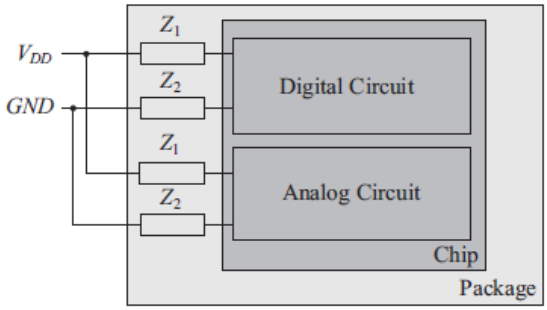

Figure 1.08: Illustration of separate power supply lines.

1.2.2 Separate Packages

One method to avoid substrate coupling is to separate the analog circuits from the digital circuits by simply placing them on separate chips in separate packages, as illustrated in Fig. 1.09. Hence, the analog circuit does not suffer from the digital switching noise that is spread through the substrate. A drawback of using separate packages is that the communication between the packages consumes a considerable amount of power. The communication between the chips is also slower compared to on-chip communication. To obtain low power consumption, the number of packages should generally be as few as possible. The mounting area on a PCB increases as well for an increased number of packages.

1.2.3 Multi-Chip Module and System-in-Package

In a multi-chip module (MCM) or a system-in-package (SiP) several silicon dies share the same package. SiP can simply be described as an MCM with a more pronounced focus on implementing a whole system in a package. In an MCM, separate silicon dies can be used for a sensitive analog circuit and a noisy digital circuit. In this way the substrate coupling is avoided. Another advantage is that the yield is larger for silicon dies of less area. In comparison with an approach using separate packages for analog and digital circuits the MCM yields lower power consumption and occupies a smaller area on a PCB. Furthermore, the communication between the chips is faster within a package than between ICs on a PCB. The MCM technique has been used in, e.g., microprocessors where memory has been placed in the same package as the processor. MCM has also been used for mixed-signal

systems such as cellular phones. The benefits are, e.g., decreased area,fast communication between chips, as well as good isolation between sensitive and noisy circuits. In Fig. 1.10 three different MCM techniques are illustrated. In Fig. 1.10(a), two chips are placed adjacent to each other and interconnected with bonding wires or solder balls and strip lines in a substrate (not to be mixed with a silicon substrate). In Fig. 1.10(b), two stacked chips are shown that are interconnected using bonding wires. In Fig. 1.10(c), three stacked chips withthrough chip interconnects are shown. In, six chips were stacked and interconnected using through chip interconnects together with small solder joints. Here, the chips have been thinned down to about 10 mm in height resulting in a package with small height.

Figure 1.09: Two chips packaged in separate packages.

1.2.4 Distance

One intuitively and straightforward approach to reduce the coupling between circuits is to place them with some extra distance in between as illustrated in Fig. 1.11. This approach is effective in lightly doped substrates where the impedance is significantly increased with distance. The cost of increasing the distance between the circuits is mainly the increased silicon area. In heavily doped substrates, increasing the distance between the circuits is inefficient as soon as the distance is more than about four times larger than the thickness of

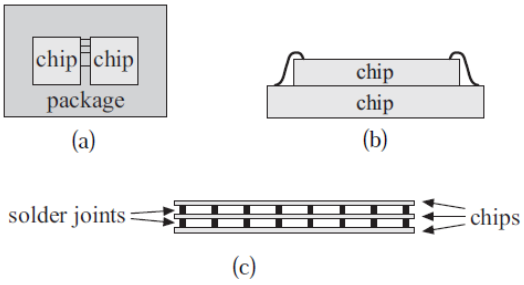

Figure 3.10: (a) Two chips in a package, (b) two stacked chips interconnected with bonding wires, and (c) three stacked chips interconnected with solder joints and through chip interconnects.

the epitaxial layer This is due to that the p+ layer has a high conductance and can therefore be approximated as a single node. Consequently, the substrate noise is approximately uniform on the entire chip area.

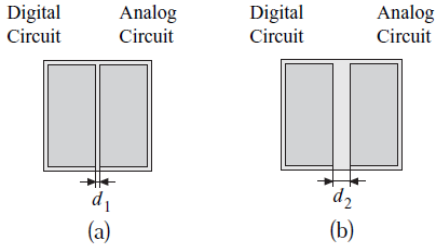

Figure 1.11: (a) Two circuits with short distance in between, and (b) two circuits with an increased distance in between.

1.2.5 Floor planning

When different circuits are integrated on the same chip there are many ways to place the circuits. The placement of the circuits affects the couplings through the substrate. Therefore, the floor plan is an important design step in mixed-signal designs where substrate noise is an issue.floor planning can be done manually, which may require a high design effort. In an automatic florplanner a larger design space can be explored. In analgorithm

for floorplanning is presented. During floorplanning there must be some information about the noise a circuit generates and how much noise a circuit can tolerate. It is normally hard for the designer to make such noise estimations in an early design phase. This problem is targeted in where an early estimation is made with the use of system C and behavior level descriptions of the circuits.With an early estimation of which circuits that are likely to be the most noisy and most sensitive to substrate noise, it is possible to make good decisions in the floorplanning in the early design phase. In Fig. 1.12, a floorplan is shown where a sensitive circuit has been placed as far as possible within the chip bounds from the noisy circuit. Areas of silicon without circuits can also be added together with guard bands to obtain less coupling. With a careful floorplanning, it is possible to minimize the receivedSubstrate noise in the sensitive circuits.

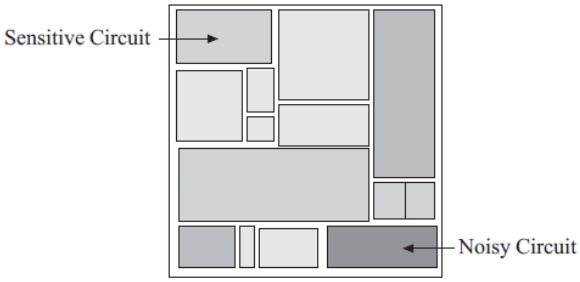

Figure 1.12: Illustration of an on-chip floorplan.

1.2.6 Silicon-on-Insulator

In a silicon-on-insulator (SOI) technology, a thin-film of silicon is placed on an insulating layer (e.g., silicon oxide) as illustrated in Fig.1.13. Beneath the insulating layer a silicon substrate is used. An advantage of a thin-film of silicon instead of a conventional bulk is the reduced parasitic pn-junctions. The lower amount of parasitic capacitance yields faster and less power consuming circuits. With an ideal isolator no substrate coupling wouldexist in the SOI technology. In reality, the isolator is not perfect, since the thin film iscapacitively coupled to the substrate. Consequently, substrate noise is effectively attenuated for low frequencies while higher frequencies are less attenuated.The efficiency of increasing the distance between the circuits in SOI depends on what type of substrate that is used. Normally, a lightly doped substrate isused, which makes it possible to increase the.

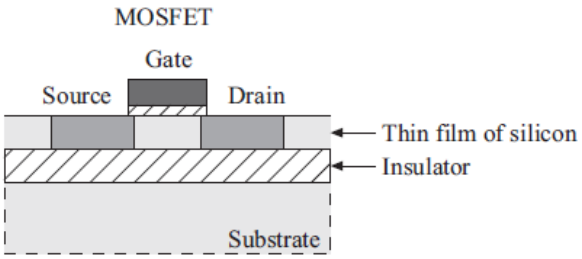

Figure 1.13: Illustration of a cross-section of a MOSFET in the silicon-on-insulator technology.

Impedance between two circuits by increasing the distance. The coupling can be effectively reduced by increasing the resistivity of the substrate. However, increasing the resistivity does not significantly reduce the coupling for frequencies above the frequency where the capacitive coupling through the substrate starts todominate. In a low resistivity substrate is used instead of a high resistivity substrate. By using a good grounding of the substrate the crosstalk through the substrate can be made lower than for a high resistivity substrate. In a test chip consisting of two square areas (mm2) separated with 200 mm distance was used. A 50 signal source and a 50 network analyzer were connected to the test chip during the measurements. One interestingconclusion is that the common medium resistivity substrates are worse than both low and high resistivity substrates considering the crosstalk through the substrate. However, it is hard to draw conclusions on how these results translate in the case with a digital circuit as the noise injector instead of the 50 signal source.

1.2.7 Guard Band

A guard ring or a guard band is intended to provide a low impedance path to the off-chip ground (or the off-chip positive supply) for the substrate currents. Substrate noise can be reduced if a guard is inserted in between a noisy circuit and a noise sensitive circuit, as illustrated in Fig. 1.14. A guard can be effective in a lightly doped substrate.
In a heavily doped substrate the effect of guard rings is limited due to that the current path is mainly through thehighly conductive p+ layer. Therefore, guard rings are ineffective for suppressing noise in heavily doped substrates. The suppression that still may occur from the use of a guard is mainly due to that the interconnect impedance between on-chip and off-chip is reduced.

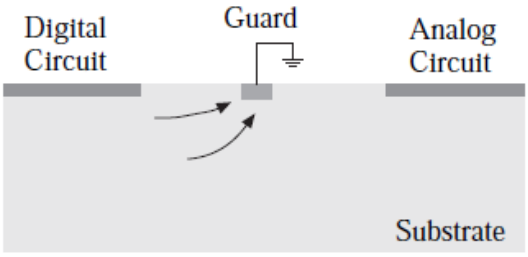

Figure 1.14: A guard placed between a digital and an analog circuit.

A similar effect is obtained if the extra pins that are dedicated for the guard are dedicated for the power supply instead.With *p*+ contacts, the guard is directly connected to the substrate. With an *n*-well as guard the substrate region surrounding the guard is capacitively coupled to either ground or the positive supply. The impedance from the substrate via the pn-junction to the *n*-well and through the *n*-well to the *n*+ contact is much higher than the impedance from the substrate through the *p*+ substrate contact. Therefore the *p*+ guard is preferable.

In CMOS processes a channel stop implant layer of about 1 mm is normally used in the top of the substrate to prevent the substrate from forming a parasitic transistor channel. The channel stop implant is highly doped and may be the main path of the substrate currents. By inserting an *n*-well in a *p* substrate the channel stop implant is interrupted by the higher resistivity of the *n*-well and the coupling is reduced. Separate package pins should be dedicated for guards, otherwise the guard may even increase the coupling between circuits. For instance, if an analog guard is located at some distance from the analog circuit and the guard is connected to the analog ground on-chip, then the noise at the location of the guard will be spread via the interconnect to ground in the analog circuit

In SOI technologies a guard band cannot be connected directly to the substrate due to the insulating layer beneath the thin-film. In SOI, guard bands consist of regions where the thin film is connected to ground as illustrated in Fig. 1.15(a). The parasitic capacitance between the thin film and the substrate is here acting as a decoupling capacitance. In paper IV, simplified comparisons between the substrate coupling in SOI and conventional bulk technology are made. With additional process steps and an increased cost in manufacturing it is possible to use guards that are directly connected to the silicon substrate beneath the insulator layer as illustrated in Fig. 1.15(b). This has been shown to be effective according to the results in.

1.2.8 Active Guard Band

In an active guard band was presented to suppress substrate noise. Here an amplifier is used to sense the substrate noise and cancel it, as illustrated in Fig. 1.18. Measurements on a test chip show that the received substrate noise is decreased from 5 mV to 1.5 mV for frequencies up to 10 kHz. Noisesuppression was observed for frequencies up to 10 MHz, with low suppression for higher frequencies. In the technique in is used resulting in noise suppression of more than 5 dB and up to 20 dB in the frequency band from 4 MHz to 200 MHz. The improved suppression for the higher frequencies is explained by the 400 MHz bandwidth of the amplifier used in to compare with lower than 10 MHz in. Hence, the efficiency of the technique depends much on the bandwidth of the amplifier.

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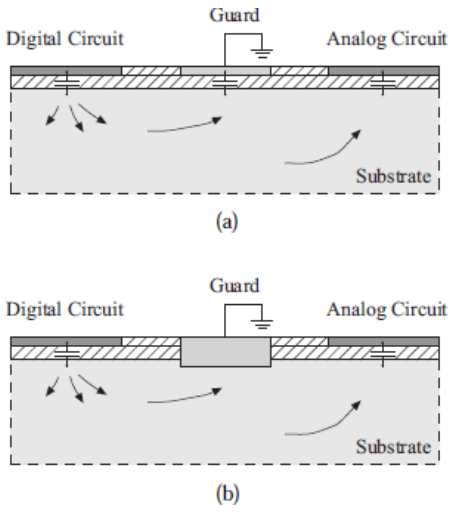

Figure 1.15: (a) Guard band in a conventional SOI, and (b) guard band in SOI with extra process steps.

The inductance is normally the dominant part of the power supply impedance and the corresponding SSN is approximately in proportion to di/dt. In di/dton the power supply line of a digital circuit is measured with the use of an on-chip inductor. The measured di/dt is used for canceling substrate noise in where an amplifier injects a current via a substrate contact (i.e., guard band) in between the digital circuit and the noise sensor. A substratenoise reduction of 30% was measured when the digital circuit had an operation frequency of 500 MHz. The power consumption of the amplifierwas 14 mW. In a guard with an active decoupling is used. The circuit is illustrated in Fig. 1.17, where the effective capacitance seen in the guard node is due to miller-effect(A+1)C, where *A* is the gain of the amplifier and *C* the capacitance in the feedback loop. Measurements on a test chip containing a shift register, showed a noise reduction of 31% with the active decoupling enabled. The shift register was operated at 200 MHz. In this case two activedecoupling circuits were used that togetherconsumed 11 mW.

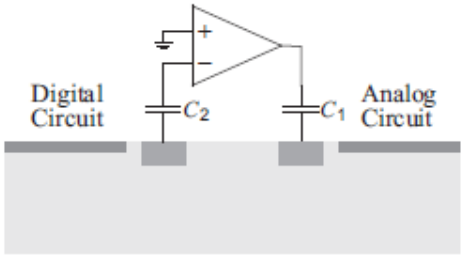

Figure 1.16: Illustration of an active guard band.

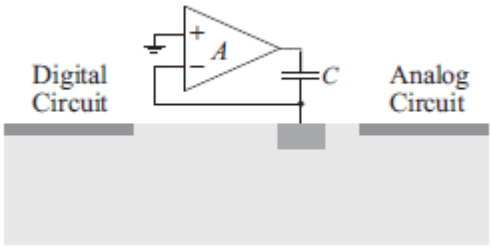

Figure 1.17: Illustration of a guard with active decoupling.

1.2.9 Deep Trench Isolation

A deep trench isolation structure consists of a trench filled with undopedpolysilicon. The trench serves as a high impedance wall in the substrate. In Fig. 1.18 an illustration of a deep trench is shown where the trench depth is 15 mm. The method has been proven to be effective up to 2 GHz in . For frequencies above 2 GHz the isolation is degraded by the capacitive coupling through the trench.

1.3 Reduction of Sensitivity to Substrate Noise

In high performance analog circuits, fully differential circuits with differential signal paths are often used. In general, differential architectures are less influenced by substrate noise than single ended architectures . A high rejection of substrate noise can be obtained with this technique if the circuit is built in a symmetrical manner. The symmetry of the circuit could in an ideal case result in that the differential paths are affected in the same way by the substrate noise. Hence, the noise is ideally eliminated since only the difference between the signals is of interest in a differential architecture. In reality there are effects that limit the rejection of the substrate noise. For example, the differential signal paths on a fabricated chip are not equal due to component mismatches.Furthermore, the noise is not injected

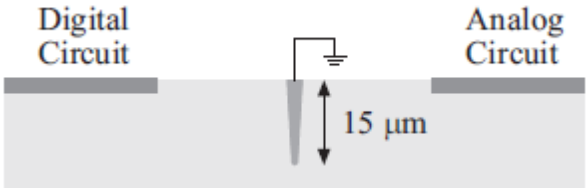

Figure 1.18: A deep trench placed between an analog and a digital circuit.

symmetricallydue to asymmetries of the layout with respect to the paths of the substrate currents. This means that differential architectures may lower the effects of the received substrate noise but not entirely eliminate them.

3. CONCLUSION

The noise generated when the test pattern generator changed outputs was found to be significant. The input pads on the chip have large capacitive coupling to the substrate and the input pads are also connected to input buffers. Therefore, a transition on an input signal results in a significant SSN. If the test pattern generator changes data at the same time as the digital circuit switches, the two respective noise contributions will interact. We present a method that separates the noise originating from the digital circuit from the noisegenerated due to the change of test vectors. This method was used when measuring the substrate noise in the digital circuit.

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